In the Claims:

1. (Currently Amended) A ferroelectric memory device including an extended memory unit, comprising:

a cell array block including a main bitline and a plurlaity of sub bitlines, the main bitline connected between a main bitline pull-up controller and a column selection controller, and each sub bitline connected to the main bitline and a unit cell;

a data bus unit connected to the column selection controller;

an input/output circuit unit including a sense amplifier array connected to the data bus unit;

an extended memory unit sharing the main bitline included in the cell array block and including a plurality of cell ~~blocks;~~ blocks; and

an extended memory controller for controlling the extended memory unit in response to an external control signal.

2. (Original) The device according to claim 1, wherein the main bitline pull-up controller is a PMOS transistor having a gate to receive a control signal, a source connected to a positive power and a drain connected to the main bitline.

3. (Original) The device according to claim 1, wherein the column selection controller is a switch having a gate to receive a control signal, a terminal connected to a main bitline and the other terminal connected to a data bus line.

4. (Original) The device according to claim 1, wherein the cell array block includes a plurality of sub cell blocks corresponding to the plurality of sub bitlines respectively, each sub cell block comprising:

a first NMOS transistor having a gate connected to a first terminal of the sub bitline and a drain connected to the main bitline;

a second NMOS transistor having a gate connected to a third control signal, a drain connected to a source of the first NMOS transistor and a grounded source;

a third NMOS transistor having a gate connected to a fourth control signal, a drain connected to a second terminal of the sub bitline and a grounded source;

a fourth NMOS transistor having a gate connected to a fifth control signal, a source connected to the second terminal of the sub bitline and a drain connected to a sixth control signal; and

a fifth NMOS transistor having a gate connected to a seventh control signal, a drain connected to the main bitline and a source connected to the second terminal fo the sub bitline.

5. (Original) The device according to claim 4, wherein the cell block included in the extended memory unit has the same structure as that of the sub cell block.

6. (Original) The device according to claim 5, wherein a part of the cell block is used as a redundancy cell region and the rest part of the cell block is used as an extended cell region.

7. (Original) The device according to claim 6, further comprising:

a redundancy decoder for driving a wordline/plateline included in the redundancy cell region when the redundancy cell region is accessed;

an extended memory decoder for driving a wordline/plateline includded in the extended cell region when the extended cell region is accessed; and

a sub bitline controller for outputting a plurality of control signals corresponding to the first to the seventh control signals commonly used in the sub cell block and the cell block.

8. (Original) The device according to claim 4, wherein the extended memory unit comprises a cell block having the same structure as that of the sub cell block,

wherein the cell block comprises smaller number of unit cells than those of the sub cell block, and a capacitor for compensating for difference in capacitance resulting from difference in the number of the unit cells, and

wherein the capacitor is connected between a sub bitline included in the cell block and ground.

9. (Original) The device according to claim 8, wherein the extended memory unit uses a part of the unit cell in the cell block as the redundancy cell region, and the rest part of the unit cell as the extended cell region.

10. (Original) The device according to claim 9, further comprising:

a redundancy decoder for driving a wordline/plateline included in the redundancy cell region only when the redundancy cell region is accessed;

an extended memory decoder for driving a wordline/plateline included in the extended cell region only when the extended cell region is accessed; and

a sub bitline controller for outputting a plurality of control signals corresponding to the first to the seventh control signals commonly used in the sub cell block and in the cell block.

11. (Original) A ferroelectric memory device including an extended memory unit, comprising:

a controller for storing a predetermined key value in response to an external command signal, for outputting an extended memory control signal corresponding to the external control signal when the external control signal satisfies a predetermined condition of the key value, and for maintaining the stored key value when power is off; and

an extended memory unit including a plurality of cells for storing predetermined data in response to the extended memory control signal, the plurality of cells sharing existing bitlines.

12. (Original) The device according to claim 11, wherein the controller comprises:

a program command decoder for decoding the external command signal and outputting a program command signal;

a power-up circuit for outputting a reset signal which is inactivated after power is turned on and stabilized;

a register controller for outputting a register control signal to control the program process when the program command signal is activated and to contol the process of readingthe program result when the reset signal is inactivated;

a register for storing a key value corresponding to a data signal supplied externally in response to the register control signal, for outputting the stored key value externally, and for maintaining the stored key value when power is off; and

an extended memory controller for controlling the extended memory unit in response to a key value outputted from the register and an external control signal.

13. (Original) The device according to claim 12, wherein the register comprises:

a first amplifier for amplifying a voltage of a node having higher voltage between first and second nodes to a positive voltage in response to a first control signal;

a second amplifier for amplifying a voltage of a node having lower voltage between the first and the second nodes to a ground voltage in response to a second control signal;

an input unit for outputting a data signal into the first and the second nodes in response to a third control signal; and

a storage unit for storing the signal outputted into the first and the second nodes in response to a fourth control signal and for maintaining the stored information when power is off.

14. (Original) The device according to claim 13, wherein the first amplifier comprises:

a first PMOS transistor having a gate to receive the first control signal and a source connected to a positive power;

a second PMOS transistor having a gate connected to the first node, a source connected to a drain of the first PMOS transistor and a drain connected to the second node; and

a third PMOS transistor having a gate connected to the second node, a source connected to the drain of the first PMOS transistor and a drain connected to the first node.

15. (Original) The device according to claim 13, wherein the second amplifier comprises:

a first NMOS transistor having a gate connected to the first node and a drain connected to the second node;

a second NMOS transistor having a gate connected to the second node and a drain connected to the first node; and

a third NMOS transistor having a gate to receive the second control signal, a drain connected to sources of the first NMOS transistor and the second NMOS transistor, and a source connected to ground.

16. (Original) The device according to claim 13, wherein the input unit comprises:

a first PMOS transistor having a gate to receive a NAND operation result of the data signal and the third control signal, a source connected to a positive power and a drain connected to the second node;

a first NMOS transistor having a gate to receive an AND operation result of the data signal and the third control signal, a source connected to ground and a drain connected to the first node;

a second NMOS transistor having a gate to receive an AND operation result of a signal having an opposite level to the data signal and the third control signal, a source connected to ground and a drain connected to the second node; and

a second PMOS transistor having a gate to receive a NAND operation result of a signal having an opposite level to the data signal and the third control signal, a source connected to a positive power and a drain connected to the first node.

17. (Original) The device according to claim 13, wherein the storage unit comprises:

a first ferroelectric capacitor having a first terminal to receive the fourth control signal and a second terminal connected to the first node;

a second ferroelectric capacitor having a first terminal to receive the fourth control signal and a second terminal connected to the second node;

a third ferroelectric capacitor having a first terminal connected to the first node and a second terminal connected to ground; and

a fourth ferroelectric capacitor having a first terminal connected to the second node and a second terminal connected to ground.

18. (Currently Amended) A ferroelectric memory device including an extended memory unit, comprising:

an ECC controller for outputting an extended memory control signal in response to a repair request signal activated when a fail cell is accessed, and for inactivating the fail cell;

an extended memory unit including a redundancy cell for replacing the fail cell; and

an extended memory controller for controlling the extended memory unit in response to the extended memory control ~~signal.~~ signal,

wherein the repair request signal is generated by an outer system when the failed cell is about to be accessed by the outer system.

19. (Original) The device according to claim 18, wherein the extended memory unit comprises:

a first extended memory unit for storing an address of the fail cell and an address of the redundancy cell corresponding to the fail cell; and

a second extended memory unit including the redundancy cell,

wherein the extended memory controller controls the redundancy cell using the address of the redundancy cell obtained from the first extended memory unit.